In the Claims

Claims 1-8, 10-25, and 34-75 are pending in the application with claims 3, 10, and 21 amended herein.

1. (previously presented) A capacitor fabrication method comprising:

forming a first capacitor electrode over a substrate;

atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode;

forming a capacitor dielectric layer over the barrier layer; and

forming a second capacitor electrode over the dielectric layer.

2. (original) The method of claim 1 wherein the atomic layer depositing occurs at a temperature of from about 100 to about 600 °C and at a pressure of from about 0.1 to about 10 Torr.

3. (currently amended) The method of claim 1 wherein the atomic layer deposited barrier layer has a thickness of from about [[50]] 200 to about 500 Angstroms.

4. (original) The method of claim 1 wherein the atomic layer deposited barrier layer contacts one of the first or second electrodes.

5. (original) The method of claim 1 wherein the atomic layer deposited barrier layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

6. (original) The method of claim 1 wherein the dielectric layer exhibits a K factor of greater than about 7 at 20 °C.

7. (original) The method of claim 1 wherein at least one of the first or second electrodes comprise polysilicon and the dielectric layer comprises oxygen.

8. (original) The method of claim 1 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

9. (cancelled).

10. (currently amended) The method of claim [[9]] 1 further comprising atomic layer depositing another conductive barrier layer to oxygen diffusion over the dielectric layer.

11. (original) The method of claim 1 wherein the forming the electrodes and the dielectric layer occur by other than atomic layer deposition.

12. (original) The method of claim 1 further comprising cleaning the first electrode prior to the atomic layer depositing by a method comprising HF dip, HF vapor clean, or NF_3 remote plasma.

13. (previously presented) A capacitor fabrication method comprising:

forming a first capacitor electrode over a substrate;

chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode;

chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by a layer of a conductive barrier material;

forming a capacitor dielectric layer over the barrier layer; and

forming a second capacitor electrode over the dielectric layer.

14. (original) The method of claim 13 wherein the first and second precursor layers each consist essentially of a monolayer.

15. (original) The method of claim 13 wherein the first and second precursor layers each comprise substantially saturated monolayers.

16. (original) The method of claim 13 wherein the first and second precursor each consist essentially of only one chemical species.

17. (original) The method of claim 13 wherein the first precursor is different from the second precursor.

18. (original) The method of claim 13 wherein the first and second precursors respectively comprise only one of the following pairs: WF_6/NH_3, $TaCl_5/NH_3$, $TiCl_4/NH_3$, tetrakis(dimethylamido)titanium/NH_3, ruthenium cyclopentadiene/H_2O, IrF_5/H_2O, organometallic Pt/H_2O.

19. (previously presented) The method of claim 13 further comprising chemisorbing additional alternating first and second precursor layers before forming the dielectric layer.

20. (original) The method of claim 19 wherein the barrier layer has a thickness and a density effective to reduce oxidation of the first electrode by oxygen from over the barrier layer.

21. (currently amended) The method of claim 19 wherein the barrier layer has a thickness of from about [[50]] 200 to about 500 Angstroms.

22. (original) The method of claim 13 wherein the barrier layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

23. (original) The method of claim 13 wherein the dielectric layer exhibits a K factor of greater than about 7 at 20 °C.

24. (original) The method of claim 13 wherein at least one of the first or second electrodes comprises polysilicon and the dielectric layer comprises oxygen.

25. (original) The method of claim 13 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

Claims 26-33 (cancelled).

34. (previously presented) A capacitor fabrication method comprising:

forming a first capacitor electrode over a substrate, the first electrode comprising silicon;

atomic layer depositing a metal-containing conductive layer over the first electrode;

forming a capacitor dielectric layer over the atomic layer deposited conductive layer; and

forming a second capacitor electrode over the dielectric layer.

35. (previously presented) The method of claim 34 wherein the atomic layer deposited conductive layer is formed on the first electrode.

36. (previously presented) The method of claim 34 wherein the atomic layer deposited conductive layer comprises elemental metal, a metal alloy, or a metal-containing compound.

37. (previously presented) The method of claim 34 wherein the atomic layer deposited conductive layer comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

38. (previously presented) The method of claim 34 wherein at least one of the first or second electrodes comprise polysilicon and the dielectric layer comprises oxygen.

39. (previously presented) The method of claim 34 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

40. (previously presented) A capacitor fabrication method comprising:

forming a first capacitor electrode over a substrate, the first electrode comprising silicon;

chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode;

chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by a layer of a metal-containing conductive material;

forming a capacitor dielectric layer over the conductive layer; and

forming a second capacitor electrode over the dielectric layer.

41. (previously presented) The method of claim 40 wherein the first and second precursor layers each consist essentially of a monolayer.

42. (previously presented) The method of claim 40 wherein the first and second precursors respectively comprise only one of the following pairs: WF_6/NH_3, $TaCl_5/NH_3$, $TiCl_4/NH_3$, tetrakis(dimethylamido)titanium/NH_3, ruthenium cyclopentadiene/H_2O, IrF_5/H_2O, organometallic Pt/H_2O.

43. (previously presented) The method of claim 40 wherein the conductive layer is formed on the first electrode, further comprising chemisorbing additional alternating first and second precursor layers before forming the dielectric layer

44. (previously presented) The method of claim 40 wherein the conductive layer comprises elemental metal, a metal alloy, or a metal containing compound.

45. (previously presented) The method of claim 40 wherein the conductive material comprises WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x.

46. (previously presented) The method of claim 40 wherein at least one of the first or second electrodes comprises polysilicon and the dielectric layer comprises oxygen.

47. (previously presented) The method of claim 40 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

48. (previously presented) The method of claim 1 wherein the substrate comprises a semiconductive wafer.

49. (previously presented) The method of claim 1 wherein the first capacitor electrode comprises HSG polysilicon.

50. (previously presented) The method of claim 49, wherein the atomic layer deposited barrier layer comprises TiN and the first capacitor electrode further comprises the TiN.

51. (previously presented) The method of claim 1 wherein the atomic layer deposited barrier layer comprises TiN.

52. (previously presented) The method of claim 1 wherein the capacitor dielectric layer comprises Al_2O_3.

53. (previously presented) The method of claim 1 wherein the second capacitor electrode comprises TiN.

54. (previously presented) The method of claim 1 wherein the first capacitor electrode comprises HSG polysilicon, the atomic layer deposited barrier layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

55. (previously presented) The method of claim 13 wherein the substrate comprises a semiconductive wafer.

56. (previously presented) The method of claim 13 wherein the first capacitor electrode comprises HSG polysilicon.

57. (previously presented) The method of claim 56, wherein the barrier layer comprises TiN and the first capacitor electrode further comprises the TiN.

58. (previously presented) The method of claim 13 wherein the barrier layer comprises TiN.

59. (previously presented) The method of claim 13 wherein the capacitor dielectric layer comprises Al_2O_3.

60. (previously presented) The method of claim 13 wherein the second capacitor electrode comprises TiN.

61. (previously presented) The method of claim 13 wherein the first capacitor electrode comprises HSG polysilicon, the barrier layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

62. (previously presented) The method of claim 34 wherein the substrate comprises a semiconductive wafer.

63. (previously presented) The method of claim 34 wherein the first capacitor electrode comprises HSG polysilicon.

64. (previously presented) The method of claim 63, wherein the atomic layer deposited conductive layer comprises TiN and the first capacitor electrode further comprises the TiN.

65. (previously presented) The method of claim 34 wherein the atomic layer deposited conductive layer comprises TiN.

66. (previously presented) The method of claim 34 wherein the capacitor dielectric layer comprises Al_2O_3.

67. (previously presented) The method of claim 34 wherein the second capacitor electrode comprises TiN.

68. (previously presented) The method of claim 34 wherein the first capacitor electrode comprises HSG polysilicon, the atomic layer deposited conductive layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.

69. (previously presented) The method of claim 40 wherein the substrate comprises a semiconductive wafer.

70. (previously presented) The method of claim 40 wherein the first capacitor electrode comprises HSG polysilicon.

71. (previously presented) The method of claim 70, wherein the conductive layer comprises TiN and the first capacitor electrode further comprises the TiN.

72. (previously presented) The method of claim 40 wherein the conductive layer comprises TiN.

73. (previously presented) The method of claim 40 wherein the capacitor dielectric layer comprises Al_2O_3.

74. (previously presented) The method of claim 40 wherein the second capacitor electrode comprises TiN.

75. (previously presented) The method of claim 40 wherein the first capacitor electrode comprises HSG polysilicon, the conductive layer comprises TiN, the capacitor dielectric layer comprises Al_2O_3, and the second capacitor electrode comprises TiN.